Department of
Mechanical Engineering
The University of Hong Kong

DEPARTMENT OF
MECHANICAL ENGINEERING
THE UNIVERSITY OF HONG KONG

## SEMINAR

# Title: Central Fabrication Laboratory- Technical sharing session – Advancements in Wafer Bonding Techniques and Technologies

**Date:** 25 April 2025 (Friday)
**Time:** 16:30 - 17:30
**Venue:** 7-34/35, Haking Wong Building, HKU

**Speaker:** Mr. Xing Shixin, Samuel
Senior Engineer, Teltec Semiconductor Pacific Ltd.

**Language:** Mandarin

**Limited seats available on a first-come first-served basis**

## Abstract:

The Central Fabrication Laboratory (CFL) is a cutting-edge cleanroom facility located at the University of Hong Kong. Its primary mission is to provide advanced fabrication facilities and expertise to enhance teaching and research activities in micro/nano fabrication. As a leading research laboratory, CFL offers open access not only to University of Hong Kong members but also to local and international institutions, researchers, and companies, with collaborations from the private sector always encouraged. The technical sharing sessions offered by CFL are designed to keep participants updated on the latest micro/nano fabrication techniques and provide valuable networking opportunities with experts from around the world.

Wafer bonding is a key process to achieve interfacial integration of two or more wafers via physical/chemical interactions, enabling 3D structure integration, device packaging, or material transfer. Common methods include direct bonding, adhesive bonding, and eutectic bonding, requiring control over surface cleanliness, roughness, and bonding pressure/temperature. Widely used in MEMS devices, power chip stacking, and 3D IC manufacturing, it enhances chip performance and integration density.

Wafer bonding, a core technology in advanced packaging, demonstrates remarkable advancement through Cu-Cu bonding: leveraging atomic-level interfacial bonding, it enables direct bonding without intermediate layers, reducing interconnection pitch to sub-1μm. This significantly minimizes RC delay and enhances thermal management efficiency. By overcoming limitations of traditional solder-based processes, Cu-Cu bonding supports heterogeneous integration of silicon-based and wide-bandgap materials, providing critical support for high-density applications like HBM (high-bandwidth memory) stacking and 3D IC multi-layer stacking (exceeding 100 layers). As a core engine for advancing beyond Moore's Law, it drives the transition from 2D planar integration to 3D vertical architecture, underpinning innovations in AI chips, advanced memory, and other cutting-edge semiconductor fields.

## Biography:

Mr. Samuel Xing is a Senior Engineer at Teltec Semiconductor Pacific Ltd with 18 years of experience in the semiconductor equipment industry. He joined Teltec in 2012 as a Field Engineer supporting semiconductor customers in North China. Samuel received training from leading semiconductor equipment manufacturers to share knowledge with Chinese customers in areas such as Failure Analysis, Reliability, and Production Quality Improvement. He also attended training at AML Company in the UK for wafer bonding machine installation and process technology. Over the past decade, Samuel has installed multiple AML wafer bonding machines in China and provided after-sales technical support.

**ALL INTERESTED ARE WELCOME**

**For further information, please contact Mr. YIP P.S. (3910 2637, psanyip@hku.hk) or Prof. Chan P.K.L. (3917 2634, pklc@hku.hk).**